* U F - 8 0 6 5 *

UF-8065
B. E. - II (Sem. III) (ECC) Examination
May / June – 2012
Digital Logic Design
(New Course)

Time : Hours] [Total Marks : **100**

Instructions : (1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :
☛ B. E. - 2 (SEM. 3) (ECC)

Name of the Subject :
☛ Digital Logic Design (New)

☛ Subject Code No. : 8 0 6 5 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

(2) All questions are compulsory.
(3) Figures to the right indicate full marks.
(4) Assume necessary data if required.
(5) Answer to the two section must be written in separate answer books.
(6) Justify your answer with proper explanation.

SECTION - I

1 (a) Answer following questions : **10**

(i) Convert $(111101100)_2$ to its octal equivalent.

(ii) Convert $(5A9.B4)_H$ to binary.

(iii) Simplify following boolean function :

$$AC+C\left(A+\bar{A}B\right)$$

(iv) Convert the given expression in standard POS form f(A,B,C) = (A+B) (B+C) (A+C)

(v) Draw logic diagram of half-subtractor.

(b) (i) Simplify the following three variables expression using Boolean algebra. **5**

$$Y = \sum m\ (1,3,5,7)$$

(ii) Reduce the following function using K-map technique. **5**

$$f(A,B,C,D) = \sum m\ (5,6,7,12,13)$$
$$+ \sum d\ (4,9,14,15)$$

2 (a) Implement Boolean Expression $Y=AB+\overline{AB}$ gate using NOR gates. 8

(b) Explain Binary Parallel adder. 7

OR

2 (a) Design 2-bit comparator using gates. 8

(b) Explain BCD to Excess-3 code converter. 7

3 Write short note on any three : 15

(i) Priority encoder

(ii) Programmable Logic Array

(iii) Magnitude comparator

(iv) Full adder

(v) Read only memory

SECTION - II

4 (a) Do as directed : 10

(i) Give the difference between 'Combination Circuit' and 'Sequential Circuit'.

(ii) Give the definition of the propagation delay.

(iii) In J-K Flip-flop output is _____, when J = 1, K = 1.

(iv) List the application of flip-flop.

(v) Give the block diagram of the sequential circuit.

(vi) What is synchronous counter ?

(vii) Give the excitation table of J-K flip flop.

(viii) In T Flip Flop Output frequency is 1/2 of its input frequency. True/False

(ix) The number of flip flop required to implement mod-7 counter are_____

(x) Give the characteristics table of D flip-flop.

(b) Attempt the following questions :

(i) Convert JK Flip-flop to SR Flip Flop and D Flip-flop to SR Flip-flop. 6

(ii) Explain serial in serial out shift register. 4

5 (a) What is time race problem ? Explain working of the 'Master-Slave' Flip Flop with timing diagram. 7

(b) Explain what is edge trigger flip-flop and its working. **7**

OR

(a) List the type of the shift register and explain bi-direction shift register. **7**

(b) Explain two bit 'ripple up counter', two bit 'ripple down counter' and two bit 'ripple up/down counter', with timing diagram. **7**

6 Write short note : (any two) **16**

(a) Explain 'Ring Counter' and 'Twisted Ring Counter' with timing diagram.

(b) Write short note on Universal shift register.

(c) Explain 'Serial-In Serial-Out' shift register and 'Serial In-Parallel Out' Shift register.
